Low-Power Silicon BJT LNA for 1.9 GHz

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***Abstract*—A two-stage 1.9-GHz monolithic low-noise amplifier (LNA) with a measured noise figure of 2.3 dB and an associated gain of 15 dB was fabricated in a standard silicon bipolar transistor array. It dissipates 5.2 mW from a 3-V supply including the bias circuitry. Input return loss and isolation are −9 and −20 dB, respectively.**

***Index Terms*— Bipolar array, low noise, low power, MMIC amplifier.**

I. Introduction

IN portable communication equipment, such as cellular phones and digital cordless phones, manufacturers are trying to replace as many discrete devices as possible with high-density IC's to be competitive in size, weight, power dissipation, and price. In a number of recent papers low-power low-noise amplifiers (LNA's) for S-band have been described [1]–[3]. These LNA's were fabricated using some sophisticated GaAs full-custom processes. The improving high-frequency performance of state-of-the-art silicon bipolar processes makes low-cost semicustom arrays with a limited choice of components a reasonable solution for radio frequency (RF) applications.

In order to demonstrate that in this letter, we present a very low-power monolithic 1.9-GHz silicon LNA which draws a total current of 1.75 mA including bias circuit.

II. Circuit Design

A schematic of the two-stage LNA is shown in Fig. 1. The circuit employs a high-gain common-emitter stage (Q1–RL) and a emitter–follower output stage (Q2–Q3). This approach eliminates the need for coupling capacitors. The current of the first stage is set by a resistive parallel feedback (R3 and R4), which is connected to the external matching inductor (L1) such that no noise degradation occurs. Thus, only a single supply voltage is required. This feedback also improves both the bias and RF stability of the amplifier. The circuit was simulated with Spice and with a linear simulator based on measured S- and noise parameter data of the active device. A good agreement between simulated and measured performance is found as shown in Fig. 2.

III. Measurements

The circuit was fabricated on a "Quickchip" transistor array with the Maxim GST-2 foundry process. Fig. 3 shows the gain and noise figure of the circuit measured with the HP8970B/HP8971C noise figure meter. The amplifier shows a rather flat frequency response of the noise figure from 700

Manuscript received October 23, 1997.

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Publisher Item Identifier S 1051-8207(98)02058-3.

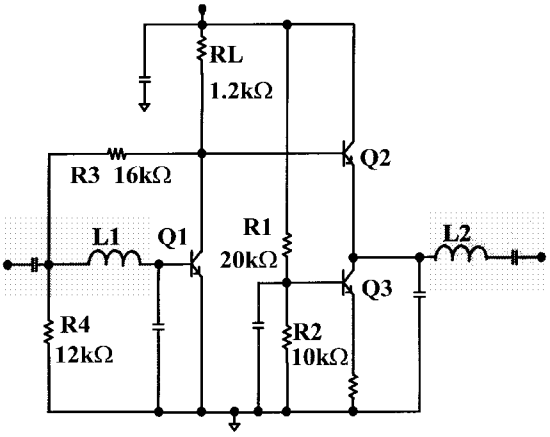

Fig. 1. Simplified schematic of the LNA (gray area: off-chip matching).

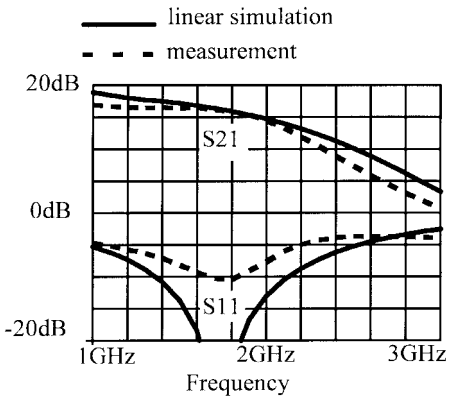

Fig. 2. Simulated versus measured gain and input return loss.

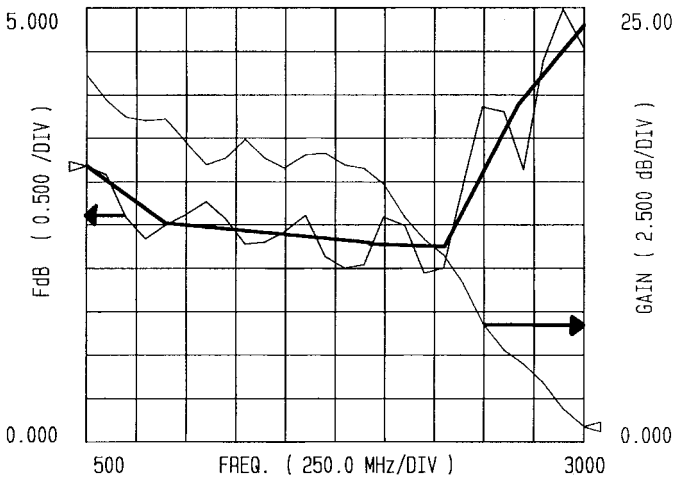

Fig. 3. Measured gain and noise figure ($V_{cc} = 3$ V, $I_{cc} = 1.75$ mA (bold line: average noise figure).

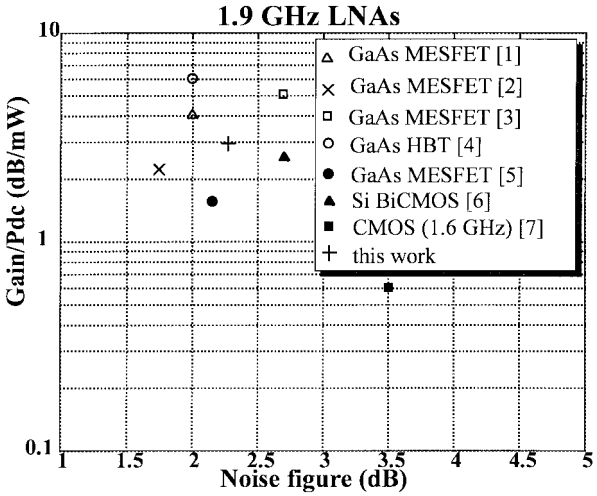

Fig. 4. Gain to DC power ratio plotted versus noise figure for several state-of-the-art L- and S-band LNA's.

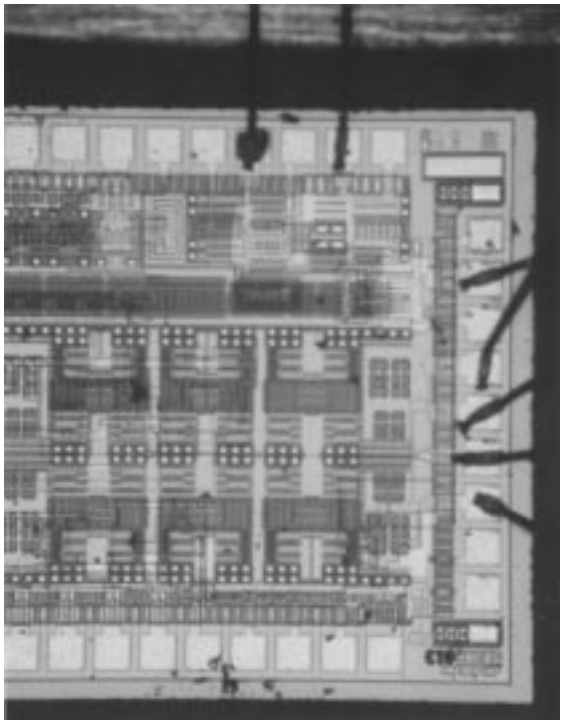

Fig. 5. Photograph of the lower right part of the 1.9×1.8 mm^2 Quickchip containing the LNA.

MHz up to 2 GHz. The best 50-Ω noise figure of 2.3 dB is achieved between 1.7 and 2.3 GHz. Note that the active device has a minimum noise figure of 1.5 dB at 1.9 GHz.

The small-signal gain is larger than 15 dB up to 2 GHz at the nominal bias of 3 V. The corresponding gain/DC-power figure of merit is 2.9 dB/mW. Compared to other L-band LNA's, this design shows low-power consumption and a competitive noise figure as seen from Fig. 4.

The noise figure is also quite insensitive to bias voltage variations. Varying the supply voltage from 2.7 to 5 V the noise figure remains between 2.2 and 2.5 dB.

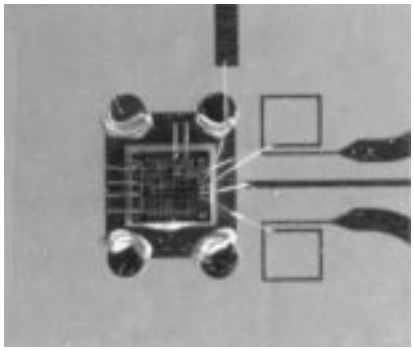

Fig. 6. Photograph of the Quickchip mounted on the test substrate. On the right are the printed inductors for input and output matching.

The designed amplifier has a measured -1 dB input compression point of -24 dBm, which equals an output compression point of -9 dBm. The third-order intermodulation intercept point is measured at -21 dBm input power. This is adequate for DECT handheld terminal.

Fig. 5 shows a photograph of the lower right part of the 1.9×1.8 mm^2 large chip containing the LNA. In Fig. 6 the chip can be seen as mounted on the substrate and bonded to the printed input and output matching inductors.

IV. Conclusion

A silicon bipolar low-power LNA for 1.9 GHz has been designed and tested. Fabricated on a semicustom transistor array, it shows a noise figure of 2.3 dB along with a 15-dB gain. The power consumption is only 5.2 mW, resulting in a high-gain/DC-power figure of merit of 2.9 dB/mW. Thus the performance degradation relative to a full custom design is minimal.

Acknowledgment

The authors wish to acknowledge Maxim for providing access to their GST-2 Quickchip technology.

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